

**Appl. No. 09/540,952
Amdt. dated August 5, 2004
Reply to Office action of April 22, 2004**

REMARKS/ARGUMENTS

In the Office action dated April 22, 2004, the Examiner rejected claims 1-4, 6-10, 14-17, 19-23, 27-30, 32-36, 38, and 39 as anticipated by Levine and rejected the remaining pending claims as obvious over Levine in view of Krishnaswamy. Applicants amend independent claims 1, 14, and 27. For the reasons provided below, Applicants believe all pending claims to be allowable.

The Examiner seems to have mainly focused on the text of column 8 of Levine. In that column, Levine states

The events to be monitored by the performance monitor 80 are selected by the event detection and control logic 170 under control of MMCR0 110 and MMCR1 120. An accurate time base 190, and a thresholder 180 that may be loaded from a control field of MMCR0 110 are also depicted. The events to be monitored by the performance monitor 80 are implementation dependent and may be performance parameters such as the number of execution unit stalls and duration, execution unit idle time, memory access time, etc. The monitor mode control registers MMCR0 110 and MMCR1 120 control the operation of the performance monitor counters PMC0 130, PMC1 140, PMC2 150, through PMC7 160.

Col. 8, lines 4-11.

Bits 10-15 of MMCR0 110 are used to store a software selectable threshold value (X), which enables a count when the threshold value is exceeded. The threshold value is exceeded when a decrementer with an initial value that equals the threshold value reaches zero before a selected event is completed. The threshold value is not exceeded when the selected event is completed before the decrementer, having an initial value that equals the threshold value, reaches zero. Bits 19-25 of MMCR0 110 are used to select the events to be monitored by PMC0 and bits 26-31 of MMCR0 110 are used to select the events to be monitored by PMC1. Similarly, MMCR1 120 bits 0-4 control the event selection for PMC2, bits 5-9 control event selection for PMC3, bits 10-14 control event selection for PMC4, bits 15-19 control event selection for PMC5, bits 20-24 control event selection for PMC6, and bits 25-28 control event selection for PMC7. There may be less than or more than eight performance monitor counters. The number of performance monitor counters is implementation dependent.

Col. 8, lines 36-55.

BEST AVAILABLE COPY

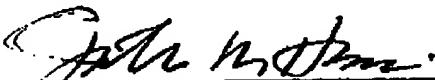
**Appl. No. 09/540,952
Amdt. dated August 5, 2004
Reply to Office action of April 22, 2004**

Applicants' independent claims require "measure[ing] a latency of execution of a particular object code instruction." The above-quoted passages from Levine does not disclose actually measuring the latency of an instruction. Levine, instead, teaches that various events can be "monitored" and that monitoring an event entails determining whether the latency of an instruction is greater than a threshold. Levine does not teach actually measuring the latency. Levine teaches starting a decrementing counter to begin counting from a threshold value towards 0. This counter either reaches 0 or is stopped before reaching 0 by a "selected event." Col. 8, lines 36-44. If the counter reaches 0, then the monitored selected event did not occur within the time counted by the counter. Ultimately, the selected event will no doubt occur, but after the counter reaches 0. Levine does not disclose actually measuring the latency of execution of the instruction. It is evidently sufficient for Levine's purposes simply to know whether an instruction takes more than a threshold amount of time to execute. Applicants contend that this is what Levine means by "monitoring" a selected event.

The Examiner also cited Krishnaswamy in an obviousness rejection of some of the dependent claims. Krishnaswamy does not satisfy the above-noted deficiency of Levine. For at least this reason, all pending claims are allowable over the art of record.

Applicants respectfully request that a timely Notice of Allowance be issued in this case. If any fees or time extensions are inadvertently omitted or if any fees have been overpaid, please appropriately charge or credit those fees to Hewlett-Packard Company Deposit Account Number 08-2025 and enter any time extension(s) necessary to prevent this case from being abandoned.

Respectfully submitted,



Jonathan M. Harris, Reg. No. 44,144
CONLEY ROSE, P.C.
(713) 238-8000 (Phone)
(713) 238-8008 (Fax)
ATTORNEY FOR APPLICANTS

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
Legal Dept., M/S 35
P.O. Box 272400
Fort Collins, CO 80527-2400

BEST AVAILABLE COPY